A

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Karl M. Robinson
Title: DEVICES HAVING IMPROVED CAPACITANCE AND METHODS OF THEIR FABRICATION
Attorney Docket No.: 303.455US2

PATENT APPLICATION TRANSMITTAL

BOX PATENT APPLICATION
Assistant Commissioner for Patents
Washington, D.C. 20231

We are transmitting herewith the following attached items and information (as indicated with an "X"):

X **DIVISIONAL** of prior Patent Application No. 08/676,708 (under 37 CFR § 1.53(b)) comprising:
- X Specification (26 pgs, including claims numbered 1 through 53 and a 1 page Abstract).
- X Formal Drawing(s) (11 sheets).
- X Copy of signed Combined Declaration and Power of Attorney (4 pgs) from prior application.
- X Incorporation by Reference: *The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied herewith, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.*
- X Check in the amount of $1,180.00 to pay the filing fee.

X Prior application is assigned of record to Micron Technology, Inc..
X Preliminary Amendment (1 pgs).
X Return postcard.

The filing fee has been calculated below as follows:

	No. Filed	No. Extra	Rate	Fee
TOTAL CLAIMS	26 - 20 =	6	x 18 =	$108.00
INDEPENDENT CLAIMS	7 - 3 =	4	x 78 =	$312.00
[ ] MULTIPLE DEPENDENT CLAIMS PRESENTED				$0.00
BASIC FEE				$760.00
TOTAL				$1,180.00

Please charge any additional required fees or credit overpayment to Deposit Account No. 19-0743.

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938, Minneapolis, MN 55402 (612-373-6900)

By: Daniel J. Kluth
Atty: Daniel J. Kluth
Reg. No. 32,146

Customer Number 21186

"Express Mail" mailing label number: EL042945488US
Date of Deposit: February 9, 1999
I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to the Assistant Commissioner for Patents, Box Patent Application, Washington, D.C. 20231.

By: Chris Hammond
Signature: Chris Hammond

S/N Unknown **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Karl M. Robinson	Examiner: Unknown
Serial No.:	Unknown	Group Art Unit: Unknown
Filed:	Herewith	Docket: 303.455US2
Title:	DEVICES HAVING IMPROVED CAPACITANCE AND METHODS OF THEIR FABRICATION	

PRELIMINARY AMENDMENT

Box Patent Application
Assistant Commissioner for Patents
Washington, D.C. 20231

Please amend the above-identified patent application as follows:

IN THE SPECIFICATION

At the first line after the title, insert therein "This is a divisional application of U. S. Serial No. 08/676,708, filed July 8, 1996."

IN THE CLAIMS

Please cancel claims 1, 7-9, 19-20, 21-28, 31, 39-49 and 53. Claims 2-6, 10-18, 29-30, 32-38 and 50-52 remain pending in the application.

Respectfully submitted,

KARL M. ROBINSON

By his Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6904

Date Feb. 9, 1999 By Daniel J. Kluth
Daniel J. Kluth
Reg. No. 32,146

CERTIFICATE UNDER 37 CFR 1.10:
"Express Mail" mailing label number: EL042945488US Date of Deposit: February 9, 1999
I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

Chris Hammond
Name

Chris Hammond
Signature

DEVICES HAVING IMPROVED CAPACITANCE AND METHODS OF THEIR FABRICATION

Background

Although there have been attempts to deposit metal oxides, such as TiO2 and SrTiO3, during semiconductor fabrication, thermal oxidation of metals in the fabrication of capacitors has been limited since an initial oxide layer prohibits further diffusion during thermal oxidation. As a result the use of high dielectric constant oxidized metals has been limited in semiconductor capacitor fabrication. One such metal, titanium dioxide, has a dielectric constant 2-15 times greater than present semiconductor capacitor dielectrics such as silicon nitride, while titanates are 2-1000 times greater.

In the January 1996 issue of Material Research, Vol. 11, No. 1, an article entitled ELECTROCHEMICAL SYNTHESIS OF BARIUM TITANATE THIN FILMS, R.R. Bacsa et al. describes the synthesizing of polycrystalline films of barium titanate on titanium substrates by the galvanostatic anodization of titanium to form a material which has a dielectric constant of 200.

Summary of the Invention

The invention includes new capacitor structures and dielectrics and methods for forming such capacitors and dielectrics.

In one exemplary embodiment the capacitor of the invention is formed by a process using only two deposition steps. The capacitor has first and second conductive plates and a dielectric is formed from the first conductive plate.

In one exemplary process in accordance with the present invention a metal layer is deposited and at least partially oxidized in an electrolytic solution. The metal oxide formed during this oxidation forms the dielectric of the capacitor. Portions not oxidized may form at least a portion of a capacitor plate.

In one exemplary implementation in accordance with the present invention, a metal layer is deposited to overlie a first capacitor plate fabricated on a semiconductor wafer. The wafer is placed in an electrolyte conducive to forming an oxide with the metal. A potential is applied across the electrolyte and the metal, and at least a portion of the metal oxidizes. In a preferred embodiment the metal is titanium and titanium dioxide is formed during the electrochemical reaction. The capacitor fabrication is completed with the formation of a second capacitor plate overlying the oxidized metal layer. The oxidized metal layer functions as the dielectric of the capacitor and has a high dielectric constant.

Brief Description of the Figures

Figure 1 is a cross section of a semiconductor wafer following the formation of a silicon dioxide layer and the masking thereof.

Figure 2 is the cross section of Figure 1 following an etch of the silicon dioxide layer and following a deposition and etch of polysilicon.

Figure 3 is the cross section shown in Figure 2 following a deposition of titanium.

Figure 4 is the cross section shown in Figure 3 when placed in an apparatus configured to perform electrochemical oxidation.

Figure 5 is the cross section shown in Figure 4 following the oxidation of the titanium layer.

Figure 6 is the cross section shown in Figure 5 following the deposition and masking of a conductive layer.

Figure 7 is the cross section shown in Figure 6 following the final capacitor formation.

Figure 8A is the cross section of the semiconductor wafer shown in Figure 1 following an etch of the silicon dioxide layer and a deposit of a first metal layer.

Figure 8B is the cross section of the semiconductor wafer shown in Figure 1 following an etch of the silicon dioxide layer and a deposit and planarization of a first metal layer.

Figure 9A is the cross section shown in Figure 8A following the electrochemical oxidation of the first metal layer and a deposit of a second metal layer.

Figure 9B is the cross section shown in Figure 8B following the planarization and electrochemical oxidation of the first metal layer and following a deposit and planarization of a second metal layer.

Figure 10A is the cross section shown in Figure 9A following an electrochemical oxidation of the second metal layer.

Figure 10B is the cross section shown in Figure 9B following a electrochemical oxidation of the second metal layer.

Figure 11A is the cross section shown in Figure 10A following the formation of a capacitor plate and the masking thereof.

Figure 11B is the cross section shown in Figure 10B following the formation of a capacitor plate and the masking thereof.

Figure 12A is the cross section shown in Figure 11A following an etch and showing one capacitor of the invention.

Figure 12B is the cross section shown in Figure 11B following an etch and showing one capacitor of the invention.

Figure 13 is a block schematic of a memory system of the invention.

Detailed Description of the Preferred Embodiments

Figures 1-7 depict cross sectionally a semiconductor wafer 1 following the process steps of a first embodiment used in fabricating the wafer 1. In Figure 1 field oxide regions 2 and wordlines 3 have been formed overlying a substrate 4 using conventional semiconductor process methods. Following the wordline formation a thick layer of silicon dioxide 5 is deposited to a thickness approximately equal to 5000 angstroms and then planarized. The silicon dioxide 5 is masked to define future capacitor substrate contact regions with mask layer 15.

In Figure 2 the silicon dioxide 5 is anisotropically dry etched to expose the substrate 4 in the unmasked regions. Following the etch a substantially conformal first conductive layer 25, preferably a polysilicon layer having a thickness of 200-400 angstroms, is deposited to overly the exposed substrate 4 and the silicon dioxide 5. Following the formation of the conductive layer 25 upper portions of the silicon dioxide layer 5 are exposed by removing portions of the conductive layer 25 using a spacer etch or using CMP (chemical mechanical planarization) following a resist deposit. The removal of portions of the conductive layer 25 creates electrically isolated portions of the conductive layer 25. The isolated portions of conductive layer 25 are first capacitor plates of the capacitor of the invention. Conventional methods for depositing the conductive layer 25 include CVD (chemical vapor deposition), PVD (pressure vapor deposition)

and electroless deposition. In an alternate embodiment a metal layer is deposited by a conventional method and functions as the first conductive layer 25.

Following the deposition and isolation of portions of the first conductive layer 25 a conformal metal layer 30 is deposited by chemical vapor deposition to overly the first conductive layer 25 and exposed portions of silicon dioxide layer 5, see Figure 3. In a preferred embodiment the conformal metal layer 30 is titanium having a thickness of approximately 16-100 angstrom. Although in this embodiment titanium is preferred other metals may be used such as copper, gold, tungsten, and nickel. In a case where metal is used as the first conductive layer 25 it may be necessary to form diffusion barrier layer or an oxidation resistant layer or both interposed between the first conductive layer 25 and the metal layers 30. Thus, it should be noted that the first conductive layer 25 may actually be comprised of more than one material. For example in a ministack application a conductive plug and further conductive layers overlying the conductive plug may form the first conductive layer.

In Figure 4 the wafer 1 is placed in electrolytic solution 34 conducive to oxidizing the metal layer 30 when a potential is applied across the electrolytic solution 34 and the metal layer 30. The electrolytic solution 34 contacts the metal layer 30. In the preferred embodiment the electrolytic solution 34 is water, such as one part NH4OH for 10 parts water or .1 Mole HCLO4. However, a basic or acidic solution could also be used. A potentiostat 36 consists of a first electrode 40, known as a counter electrode, and a second electrode 45, known as a reference electrode. Both the first 40 and second 45 electrodes are emersed in the electrolytic solution 34. The potentiostat 36 also provides a third electrode 46, known as the working electrode, which is connected to the substrate 4. The substrate 4 is in electrical communication with the metal layer 30. The potentiostat 36 is a standard device, one of which is a PAR available from E.G.& G. of Princeton, New Jersey. The preferred reference electrode is an SCE (saturated calomel electrode). The potentiostat 36 monitors the current flowing between the first and third electrodes 40 and 46. The potentiostat controls the potential between the second and third electrodes 45 and 46. Preferably, the potential is in the range of -2.0 volts to 5 volts (i.e. SCE

reference electrode) for 5-120 sec depending on the desired thickness of the dielectric. The current is measured between electrodes 40 and 46 and is controlled by varying the potential between the second and third electrodes 45 and 46 to obtain the desired current. The potentiostat allows the potential to be adjusted within a range of potentials conducive to the oxidizing of titanium. The oxidation reaction simultaneously oxidizes the metal layer 30 across the entire wafer surface.

Although in the preferred embodiment a three electrode potentiostat controls the electrochemical oxidation process, a two electrode rheostat control device may also be used. However, the oxidation is less controllable using the two electrode rheostat. When using the rheostat the second electrode 45 is eliminated and the electrochemical reaction changes the counter electrode chemistry. When this happens the potential changes. Thus the oxidation of the metal layer 30 is uncontrolled. In the three electrode preferred embodiment the existence of the reference electrode provides better control of the oxidation process.

In the first embodiment substantially all of the metal layer 30 is oxidized during the electrolytic process to form a metal oxide 35, titanium dioxide in the preferred embodiment, see Figure 5. The titanium dioxide has a high dielectric constant. Preferably, the thickness of the metal oxide ranges between 10-1000 Angstroms and the dielectric constant is between 86 and 170.

Following the oxidation step the metal oxide is chemically mechanically planarized and a second conductive layer 55 is deposited to overlie the metal silicon dioxide layer 5, the silicon oxide 50 and the metal oxide 35, see Figure 6. The second conductive layer 55 is created using conventional methods such as CVD, PVD, or electroless deposition. In the preferred embodiment the conductive layer 55 is polysilicon although metal may be used instead of polysilicon, and more than one material may be used to form conductive layer 55. A mask 60 is then formed to define the future capacitor structures.

In Figure 7 the conductive layer 55 has been etched in unmasked regions to complete the capacitor structures 65. The capacitors 65 made by the method of the invention comprises a first capacitor plate which is first conductive layer 25, a second capacitor plate which is the second conductive layer 55, and a dielectric which is the metal oxide 35.

In an alternate embodiment it is only necessary to oxidize a portion of the metal layer 30 to create a metal/ metal oxide layer, or in the preferred embodiment a titanium/titanium dioxide layer. In this case the unoxidized metal layer 30 and the polysilicon layer 25 form the first capacitor plate while the thin layer of titanium oxide forms the dielectric.

In a still further alternate embodiment multiple layers of metal are deposited and at least a portion of each metal layer is electrochemically oxidized prior to the deposition of a subsequent metal layer. In this case the dielectric comprises alternate layers of oxide and metal. In this embodiment the second conductive layer 55 is deposited on the last metal oxide created.

In a second embodiment of the invention, shown in Figures 8A-12B, a first metal layer 75, such as titanium, is sputter deposited to overly the silicon dioxide layer 5 and to contact exposed portions of substrate 4 following the etch of the silicon dioxide layer 5 shown in Figure 1. The wafer 1 is then placed in an electrolytic solution of acidic water. A current flows in the electrolytic solution in response to a potential applied across the electrolytic solution. The current is controlled with a potentiostat in order to control the oxidation of the metal layer. By controlling the oxidation it is possible to oxidize only a top portion of the first metal layer 75 to form a first metal oxide 80, see Figures 9A.

Alternately the metal layer 75 is planarized to expose the silicon dioxide prior to oxidation and formation of the first metal oxide 80, see Figures 8B and 9B.

Following the first oxidation a second metal layer 85, Figure 9A, is sputter deposited to overlie the first metal oxide 80. Again the wafer 1 is placed in the electrolytic solution and an

upper portion of the second metal layer 85 is oxidized to form a second metal oxide 90, see Figures 10A and 10B.

In the alternate embodiment, shown in Figures 9B and 10B, the second metal layer 85 has been planarized to expose the silicon dioxide prior to oxidation.

Following the oxidation of the second metal layer 85 a third metal layer 95 is sputter deposited to overly the second metal oxide layer 90, and capacitors are defined by a mask 100, see Figures 11A and 11B.

Exposed first, second and third metal layers 75, 85, and 95 and exposed first and second metal oxide layers 80 and 90 are etched to form the capacitors 105 of the invention, see Figures 12A and 12B. First and third metal layers 75 and 95 form first and second capacitor plates of the capacitors 105, and the first and second metal oxide layers 80 and 90 and second metal layer 85 form the dielectric of the capacitors 105. In a preferred embodiment the first, second, and third metal layers 75, 85, and 95 are titanium. Therefore in the preferred embodiment the metal oxide layers 80 and 90 are titanium dioxide. It is also possible to use only one or to use more than the number of metal/metal oxide layers described above as the dielectric layer, or it is possible to oxidize an entire metal layer if it is not the first or last metal layer deposited.

In further conceived embodiments the metal layer 30 (in this embodiment titanium) may be alloyed with a material, such as Strontium. In this case SrTiO3 is formed during the oxidation performed by the method of the invention. Other titanates may also be formed depending on the alloy used in combination with titanium. For Example, Ba or Pb may be combined with Ti to form BaTiO3 and PbTiO3, respectively, during oxidation. The process also works for $TiO3^{-2}$ complexes. In a still further embodiment the metal layer 30 (in this embodiment titanium) may be oxidized in a supersaturated Sr^{+2} solution such as Sr(OH)2 to form SrTrO3, in a preferred embodiment.

The capacitors 65 and 105 shown in Figures 7 and 12(A&B) respectively are typically used in a monolithic memory device 110, such as a dynamic random access memory device, as shown in Figure 13. The monolithic memory device 110 and a processor 115 form part of a memory system 120. The processor 115 is typically used to generate external control signals which accesses the monolithic memory device 110 either directly or through a memory controller.

It will be evident to one skilled in the art that many different combinations of materials, deposits and etch steps may be used to fabricate the capacitor and dielectric of the invention without departing from the spirit and scope of the invention as claimed. The method for forming the dielectric of the invention is equally applicable to any type of capacitor structure, such as trench, container, and stacked and ministacked or variations thereof. The following patents: U.S. Patent Nos. 5,438,011 (Blalock et al.), 5,097,381 (Vo), 5,155,057 (Dennison et al.), 5,321,649 (Lee et al.), 5,196,364 (Fazan et al.), 5,381,302 (Sandhu et al.), 5,392,189 (Fazan et al.), 5,082,797 (Chan et al.), 5,134,085 (Gilgen et al.), 5,354,705 (Mathews et al.), 5,049,517 (Liu et al.), 5,053,351 (Fazan et al.), 5,061,650 (Dennison et al.), 5,168,073 (Gonzalez et al.), 5,192,703 (Lee et al), 5,262,343 (Rhodes et al.), 5,234,856 (Gonzalez), and 5,416,348 (Jeng) pertaining to the fabrication of capacitors are herein incorporated by reference. Therefore the invention is only limited by the claims.

What is claimed is:

1. A method for forming a capacitor dielectric on a semiconductor substrate assembly, comprising the following steps:

providing said semiconductor substrate assembly;

forming a metal capacitor plate on said substrate assembly; and

oxidizing a portion of said metal capacitor plate to form a dielectric.

2. A method for forming a capacitor, comprising the following steps:

forming a metal capacitor plate on a substrate assembly; and

forming a dielectric from a portion of the capacitor plate.

3. The method as specified in Claim 2, further comprising the step of forming a further capacitor plate overlying the dielectric.

4. The method as specified in Claim 3, wherein said step of forming the capacitor plate comprises depositing a material to form the capacitor plate.

5. The method as specified in Claim 2, further comprising oxidizing the portion of the capacitor plate to form the dielectric.

6. The method as specified in Claim 2, further comprising the step of applying a potential across an electrolytic solution and the metal capacitor plate to oxidize said metal capacitor plate.

7. A method for forming a dielectric layer, comprising the following steps:

forming a metal layer overlying a starting substrate; and

applying a potential across an electrolytic solution and the metal layer to form the dielectric.

8. The method as specified in Claim 7, further comprising the step of oxidizing at least a portion of the metal layer to form an oxidized layer in response to said step of applying, said oxidized layer forming at least a portion of the dielectric layer.

9. A method for forming a dielectric layer, comprising the following steps:

forming a metal layer overlying a starting substrate;

applying a potential across the metal layer; and

oxidizing at least a portion of the metal layer to form an oxidized layer in response to said step of applying, said oxidized layer forming at least a portion of the dielectric layer.

10. A method for fabricating a wafer, comprising the following steps:

forming a metal layer overlying a starting substrate; and

applying a potential across an electrolytic solution and the metal layer.

11. A method of fabricating a wafer, comprising the following steps:

forming a metal layer overlying a starting substrate;

contacting the metal layer with an electrolytic solution;

applying a potential across the electrolytic solution and the metal layer; and

oxidizing at least a portion of the metal layer in response to said step of applying to form an oxidized layer.

12. The method specified in Claim 11, further comprising forming a capacitor plate overlying the starting substrate prior to said step of forming the metal layer, said metal layer overlying said capacitor plate.

13. The method as specified in Claim 11, further comprising forming a capacitor plate overlying the oxidized layer.

14. The method as specified in Claim 11, wherein a non-oxidized portion of the metal layer forms at least a portion of a capacitor plate.

15. The method as specified in Claim 11, wherein said step of applying further comprises:

connecting a first electrode in contact with the electrolytic solution to a first terminal of a potential source; and

connecting the starting substrate to a second terminal of the potential source.

16. The method as specified in Claim 15, further comprising:

positioning a second electrode to contact the electrolytic solution; and

connecting the second electrode to the potential source.

17. The method as specified in Claim 11, further comprising the step of adjusting the potential across the electrolytic solution to control the oxidation of the metal layer.

18. The method as specified in Claim 17, further comprising:

monitoring a current in the electrolytic solution; and

adjusting the potential of the electrolytic solution to maintain a desired amount of the current.

19. A capacitor, comprising:

a first conductive plate;

a second conductive plate; and

a dielectric interposed between said first and second conductive plates, wherein said dielectric is an oxide of a material of the first conductive plate.

20. A memory system, comprising:

a monolithic memory device, comprising a capacitor, wherein the capacitor comprises:

a first conductive plate;

a second conductive plate; and

a dielectric interposed between said first and second conductive plates, wherein said dielectric is an oxide of a material of the first conductive plate; and

a processor configured to access the monolithic memory device.

21. A method for forming a dielectric layer, comprising the following steps:

forming a metal layer overlying a starting substrate;

contacting the metal layer with an electrolytic solution;

applying a potential across the electrolytic solution and the metal layer; and

oxidizing at least a portion of the metal layer to form an oxidized layer in response to said step of applying, said oxidized layer forming at least a portion of the dielectric layer.

22. The method as specified in Claim 21, further comprising the step of forming a capacitor plate overlying the starting substrate prior to said step of forming the metal layer.

23. The method as specified in Claim 21, further comprising the step of forming a capacitor plate overlying the oxidized layer.

24. The method as specified in Claim 21, wherein a non oxidized portion of the metal layer forms a capacitor plate.

25. The method as specified in Claim 21, wherein said step of applying comprises the following steps:

connecting a first electrode in contact with a surface of the electrolytic solution to a first terminal of a potential source; and

connecting the starting substrate to a second terminal of the potential source.

26. The method as specified in Claim 25, further comprising the following steps:

positioning a third electrode to contact the electrolytic solution; and

connecting the third electrode to a third terminal of the potential source.

27. The method as specified in Claim 21, wherein said step of applying comprises the step of adjusting the potential across the electrolytic solution to control the oxidation of the metal layer.

28. The method as specified in Claim 21, further comprising the following steps:

monitoring a current in the electrolytic solution; and

adjusting the potential of the electrolytic solution to maintain a desired amount of the current.

29. A method for forming a capacitor, comprising the following steps:

forming a first electrically conductive layer;

forming a metal layer overlying the first electrically conductive layer;

contacting the metal layer with an electrolytic solution;

applying a potential across the electrolytic solution and the metal layer; and

oxidizing at least a portion of the metal layer to form an oxidized layer in response to said step of applying, said oxidized layer forming at least a portion of a dielectric layer of the capacitor, the electrically conductive layer forming a lower capacitor plate.

30. The method as specified in Claim 29, further comprising forming a further electrically conductive layer overlying the dielectric layer to form an upper capacitor plate.

31. A method for forming a capacitor dielectric layer, comprising the following steps:

forming a metal layer overlying at least a portion of a starting substrate;

contacting the metal layer with an electrolytic solution;

applying a potential across the electrolytic solution and the metal layer;

conducting current in the electrolytic solution in response to said step of applying; and

oxidizing at least a portion of the metal layer to form a metal oxide in response to said step of conducting current, the metal oxide forming at least a portion of the capacitor dielectric layer.

32. A method for forming a capacitor, comprising the following steps:

forming a metal layer in contact with a starting substrate;

contacting the metal layer with an electrolytic solution;

applying a potential across the electrolytic solution and the metal layer;

conducting current in the electrolytic solution in response to said step of applying; and

oxidizing a portion of the metal layer to form a metal oxide in response to said step of conducting current, the metal oxide being the capacitor dielectric, an unoxidized portion of the metal layer being a first capacitor plate.

33. The method as specified in Claim 32, further comprising the step of forming a second capacitor plate overlying the capacitor dielectric.

34. The method as specified in Claim 32, wherein the metal layer is an initial metal layer and wherein the electrolytic solution is an initial electrolytic solution and wherein the metal oxide is an initial metal oxide, and further comprising the following steps:

forming a further metal layer to overly the initial metal oxide;

contacting the further metal layer with a further electrolytic solution;

applying a potential across the further electrolytic solution and the further metal layer;

conducting current in the further electrolytic solution in response to said step of applying a potential across the further electrolytic solution; and

oxidizing, in response to said step of conducting current, at least a portion of the further metal layer to form a further metal oxide, the further metal oxide forming a further portion of the capacitor dielectric.

35. The method as specified in Claim 34, further comprising the step of forming a second capacitor plate overlying the capacitor dielectric.

36. The method as specified in Claim 34, wherein the further electrolytic solution and the initial electrolytic solution are the same solution.

37. A method for forming a capacitor, comprising the following steps:

forming an insulative layer overlying a substrate;

masking the insulative layer to define a region in which to fabricate the capacitor;

removing the insulative layer in an unmasked region to expose the substrate;

depositing a polysilicon layer overlying the insulative layer and the substrate and contacting the substrate;

removing portions of the polysilicon layer to expose the insulative layer;

chemical vapor depositing a metal layer to overly the polysilicon layer and the insulative layer;

contacting the metal layer with an electrolytic solution;

applying an electrical potential to the electrolytic solution and the metal layer; and

oxidizing, in response to said step of applying, at least a portion of the metal layer to form a metal oxide to function as a dielectric layer.

38. The method as specified in Claim 37, further comprising forming a conductive layer overlying the metal oxide layer.

39. A dielectric layer formed by the process, comprising:

forming a metal layer overlying a starting substrate;

contacting the metal layer with an electrolytic solution;

applying a potential across the electrolytic solution and the metal layer; and

oxidizing at least a portion of the metal layer to form an oxidized layer in response to said step of applying, said oxidized layer forming at least a portion of the dielectric layer.

40. The dielectric layer as specified in Claim 39, further comprising forming a capacitor plate overlying the starting substrate prior to said step of forming the metal layer, said metal layer overlying said capacitor plate.

41. The dielectric layer as specified in Claim 39, wherein a non oxidized portion of the metal layer forms at least a portion of a capacitor plate.

42. The dielectric layer as specified in Claim 39, further comprising:

connecting a first electrode in contact with the electrolytic solution to a first terminal of a potential source; and

connecting the starting substrate to a second terminal of the potential source.

43. The dielectric layer as specified in Claim 42, further comprising:

positioning a second electrode to contact the electrolytic solution; and

connecting the second electrode to the potential source.

44. The dielectric layer as specified in Claim 39, further comprising the step of adjusting the potential across the electrolytic solution to control the oxidation of the metal layer.

45. The dielectric layer as specified in Claim 39, further comprising:

monitoring a current in the electrolytic solution; and

adjusting the potential of the electrolytic solution to maintain a desired amount of the current.

46. A capacitor formed by a process, comprising:

forming a first capacitor plate;

forming a metal layer overlying the first capacitor plate;

contacting the metal layer with an electrolytic solution;

applying a potential across the electrolytic solution and the metal layer; and

oxidizing at least a portion of the metal layer to form an oxidized layer in response to said step of applying, said oxidized layer forming at least a portion of a dielectric layer of the capacitor.

47. The capacitor as specified in Claim 46, further comprising forming a conductive layer overlying the oxidized metal layer to form a second capacitor plate.

48. A capacitor formed by a process, comprising:

forming an insulative layer overlying a substrate;

masking the insulative layer to define a region in which to fabricate the capacitor;

removing the insulative layer in an unmasked region to expose the substrate;

depositing a polysilicon layer overlying the insulative layer and the substrate and contacting the substrate;

removing portions of the polysilicon layer to expose an upper surface of the insulative layer;

depositing a metal layer to overly the polysilicon layer;

contacting the metal layer with an electrolytic solution;

applying an electrical potential to the electrolytic solution and the metal layer;

oxidizing, in response to said step of applying, at least a portion of the metal layer to form a metal oxide to function as a dielectric layer; and

forming an electrically conductive layer overlying the metal oxide.

49. The capacitor as specified in Claim 48, further comprising forming a conductive layer overlying the metal oxide.

50. A method of forming a capacitor comprising only two deposition steps.

51. The method as specified in Claim 50, further comprising:

forming a first capacitor electrode during a first deposition step; and

forming a second capacitor electrode during a second deposition step.

52. The method as specified in Claim 51, further comprising forming a dielectric layer from said first capacitor electrode.

53. A capacitor comprising:

a first capacitor electrode;

a dielectric layer formed from said first capacitor electrode; and

a second capacitor electrode.

DEVICES HAVING IMPROVED CAPACITANCE AND METHODS OF THEIR FABRICATION

ABSTRACT

A capacitor formed by a process using only two deposition steps and a dielectric formed by oxidizing a metal layer in an electrolytic solution. The capacitor has first and second conductive plates and a dielectric is formed from the first conductive plate.

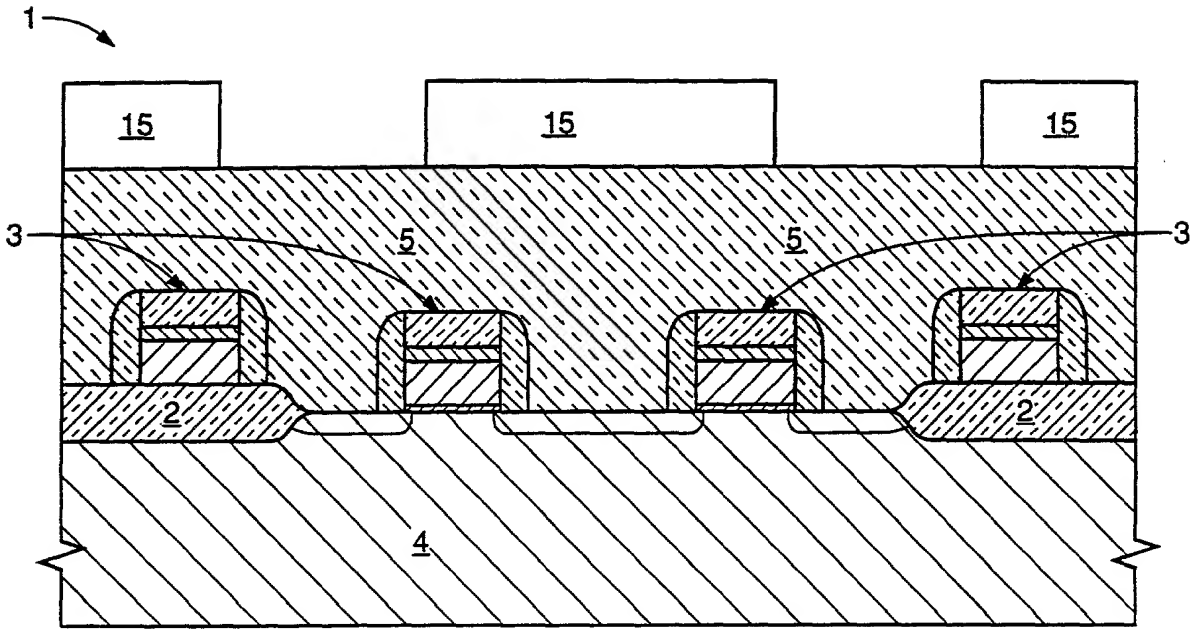

FIG. 1

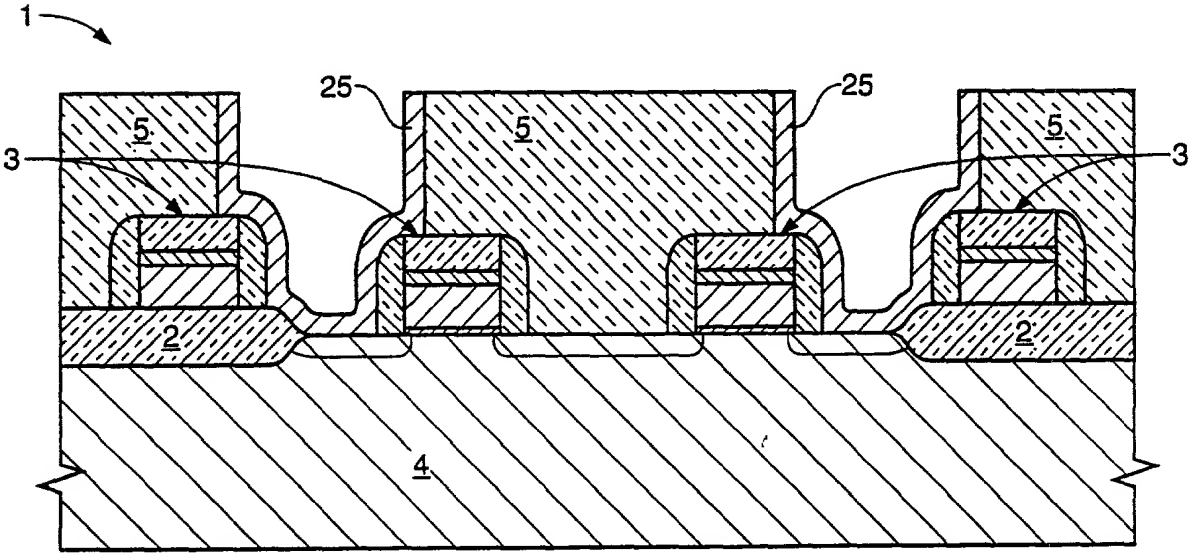

FIG. 2

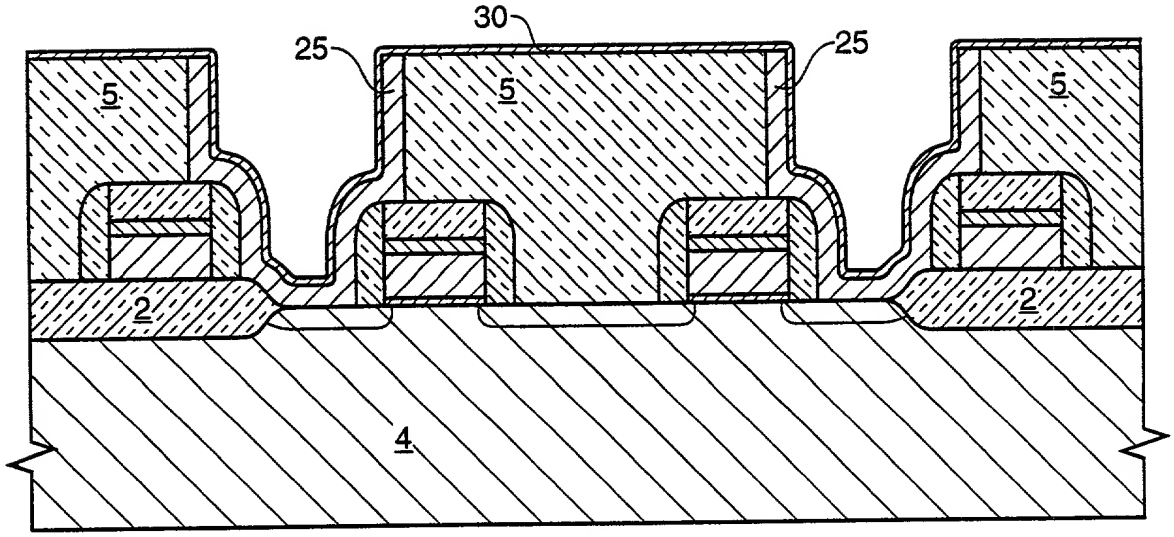

FIG. 3

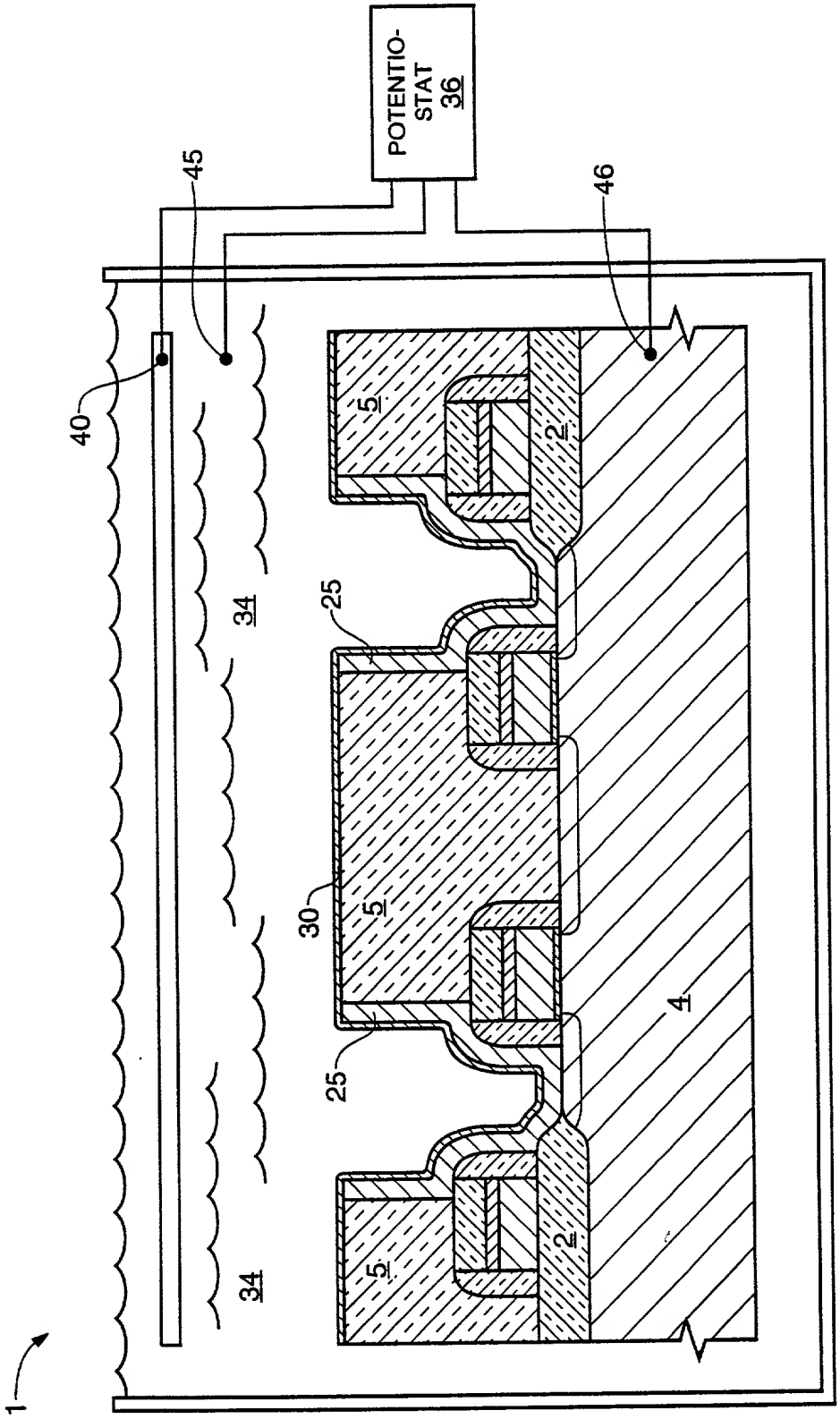

FIG. 4

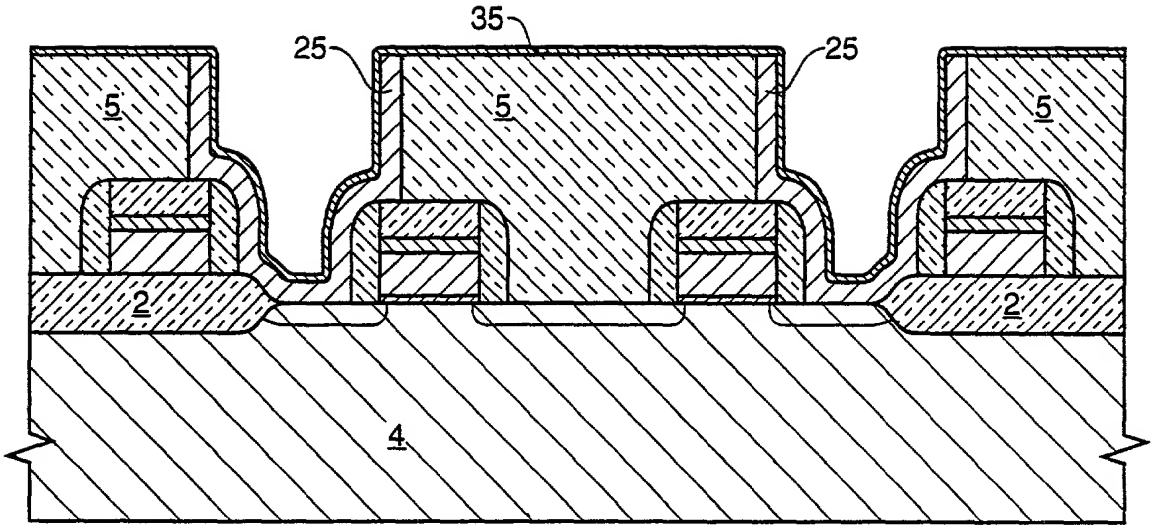

FIG. 5

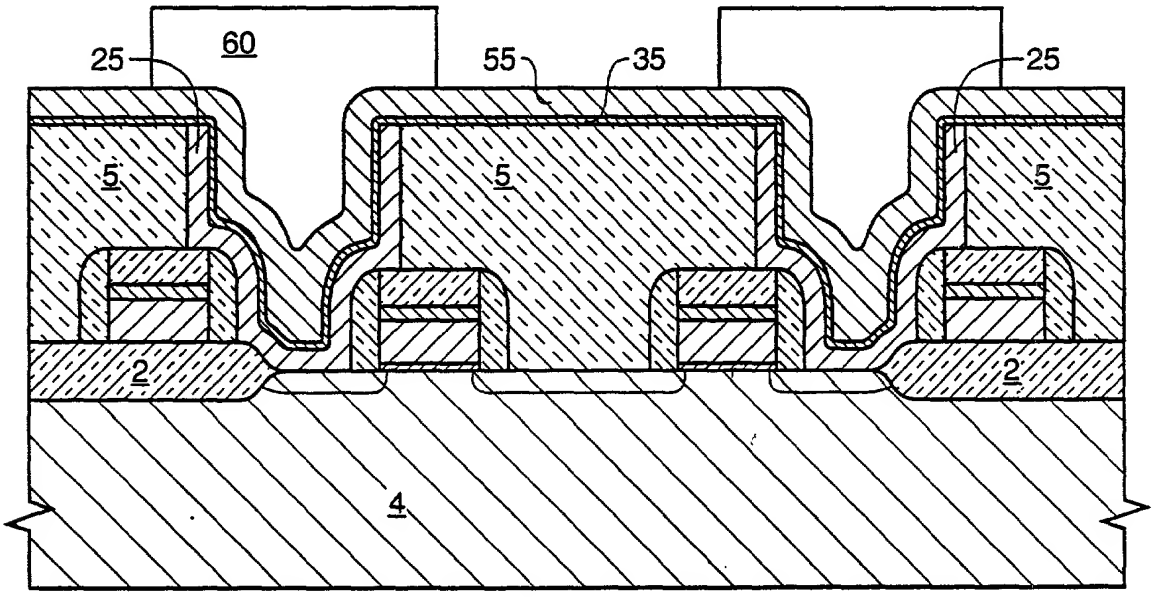

FIG. 6

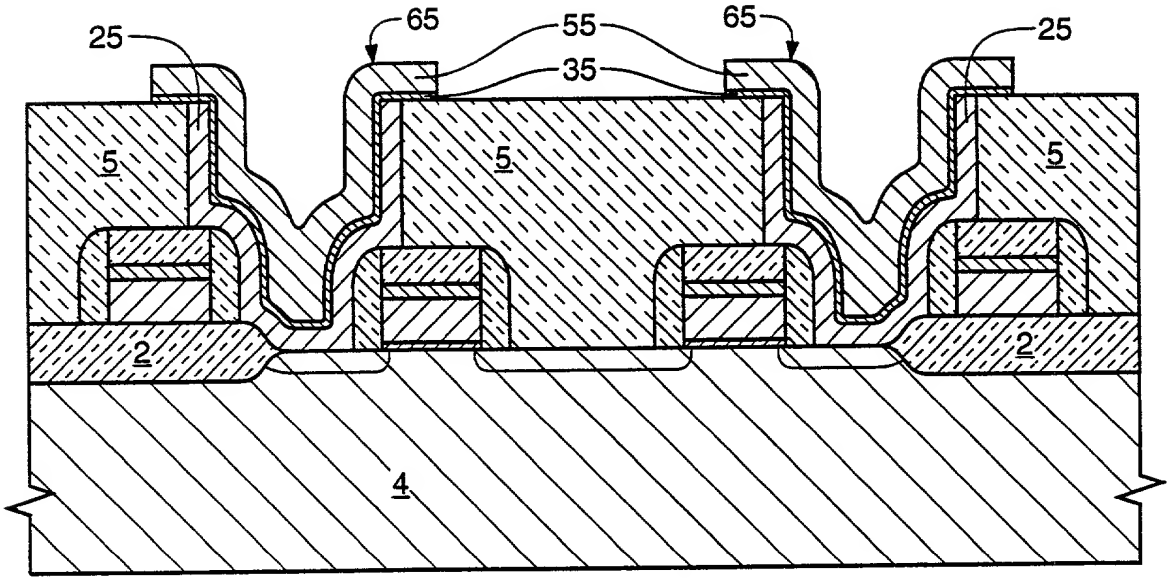

FIG. 7

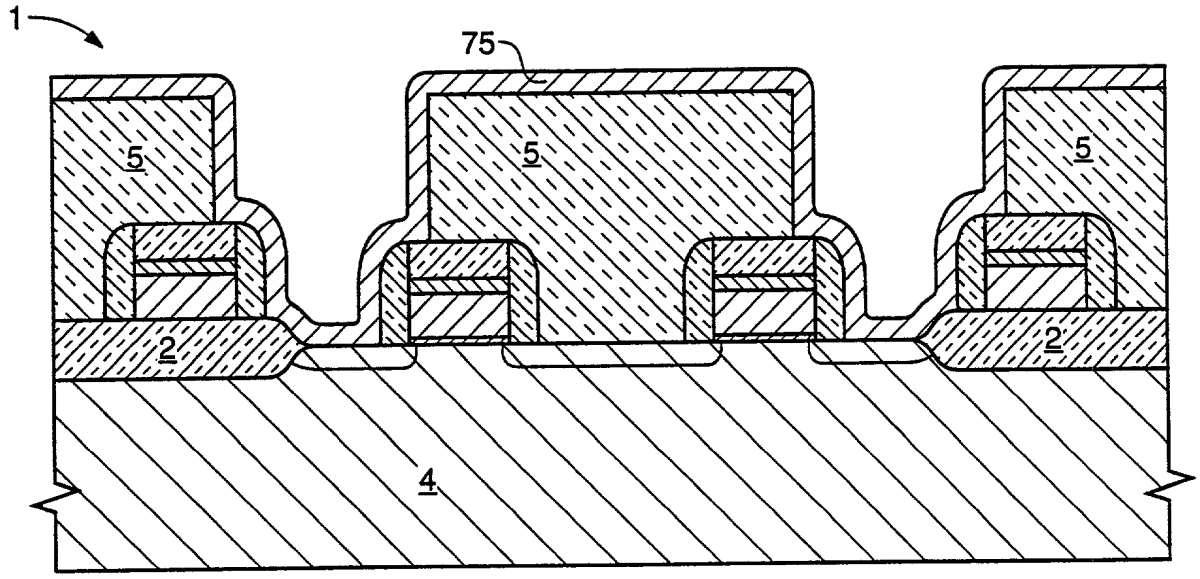

FIG. 8A

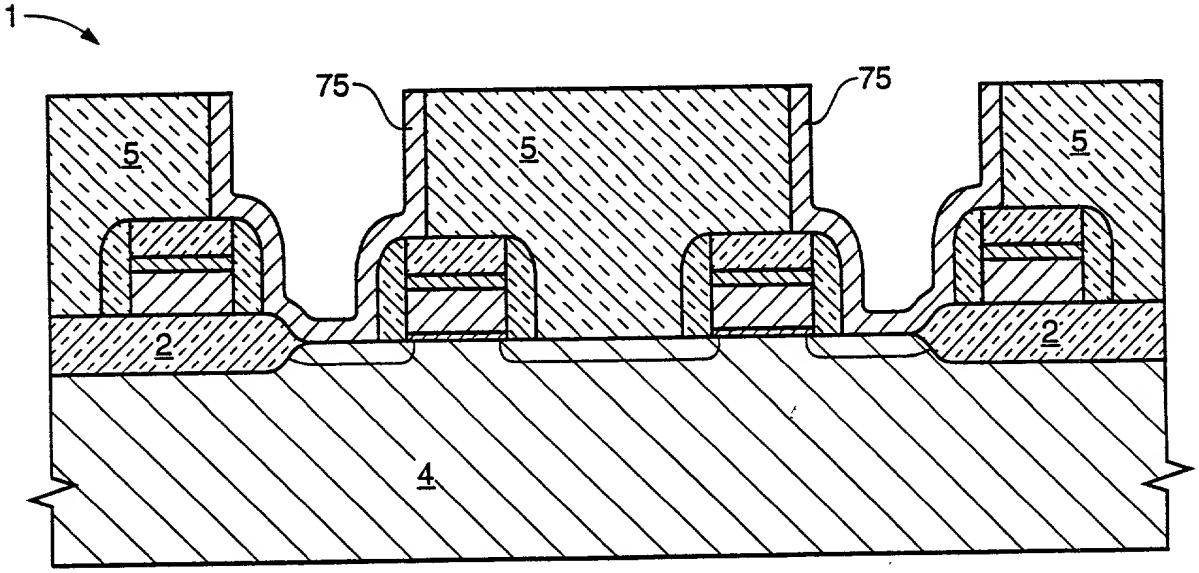

FIG. 8B

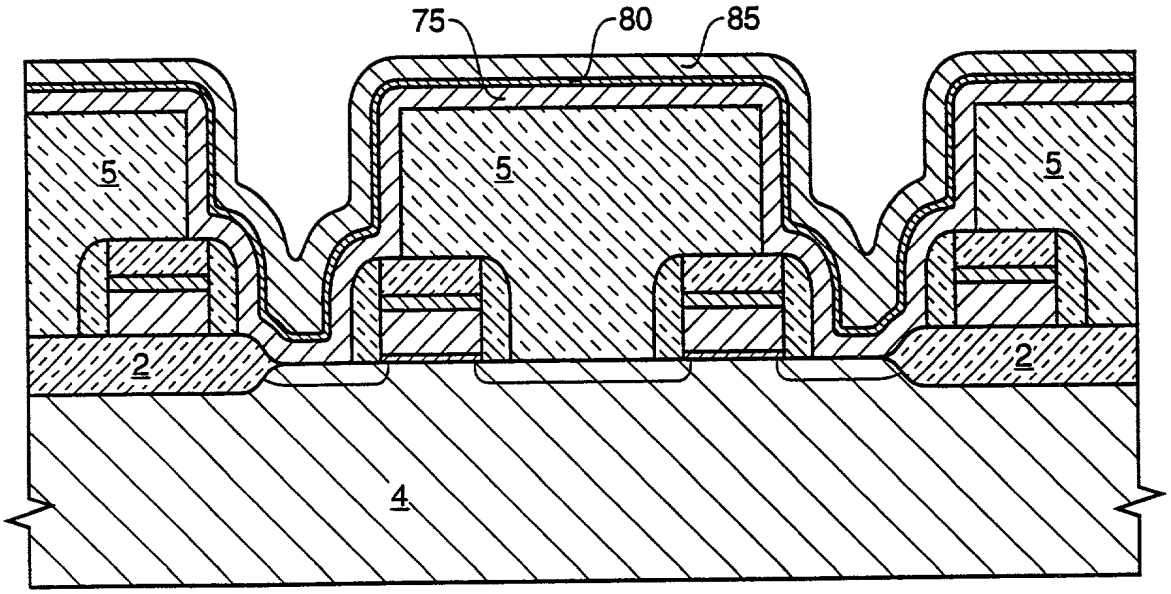

FIG. 9A

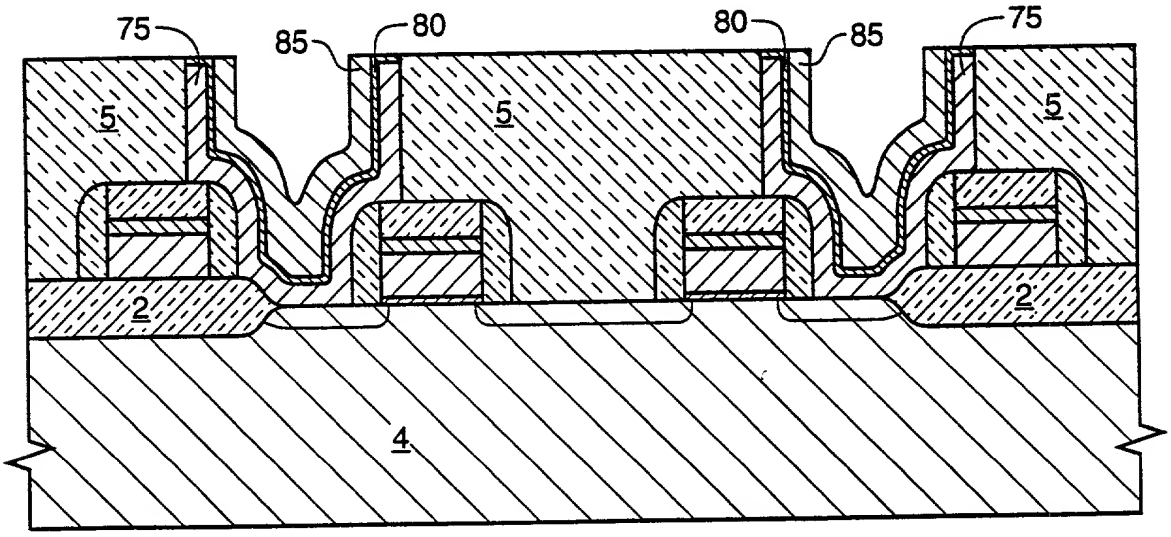

FIG. 9B

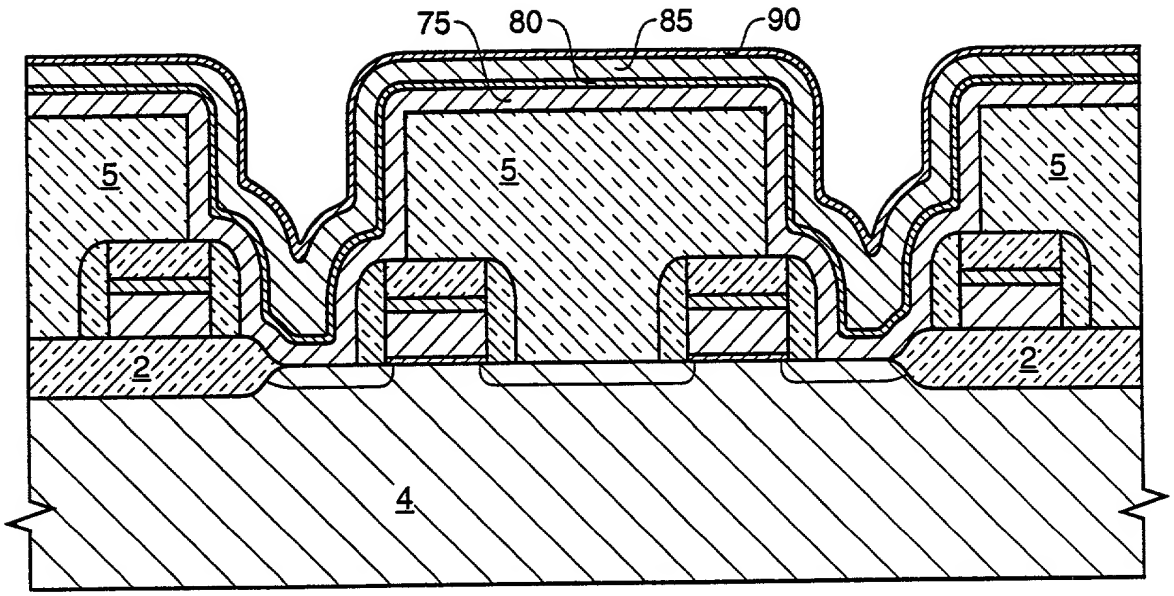

FIG. 10A

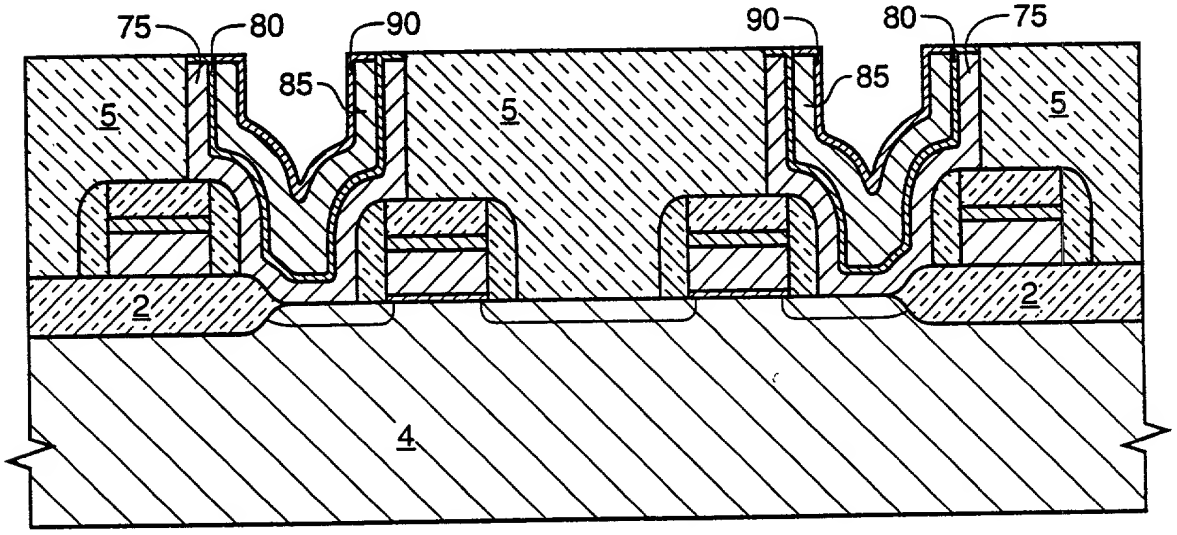

FIG. 10B

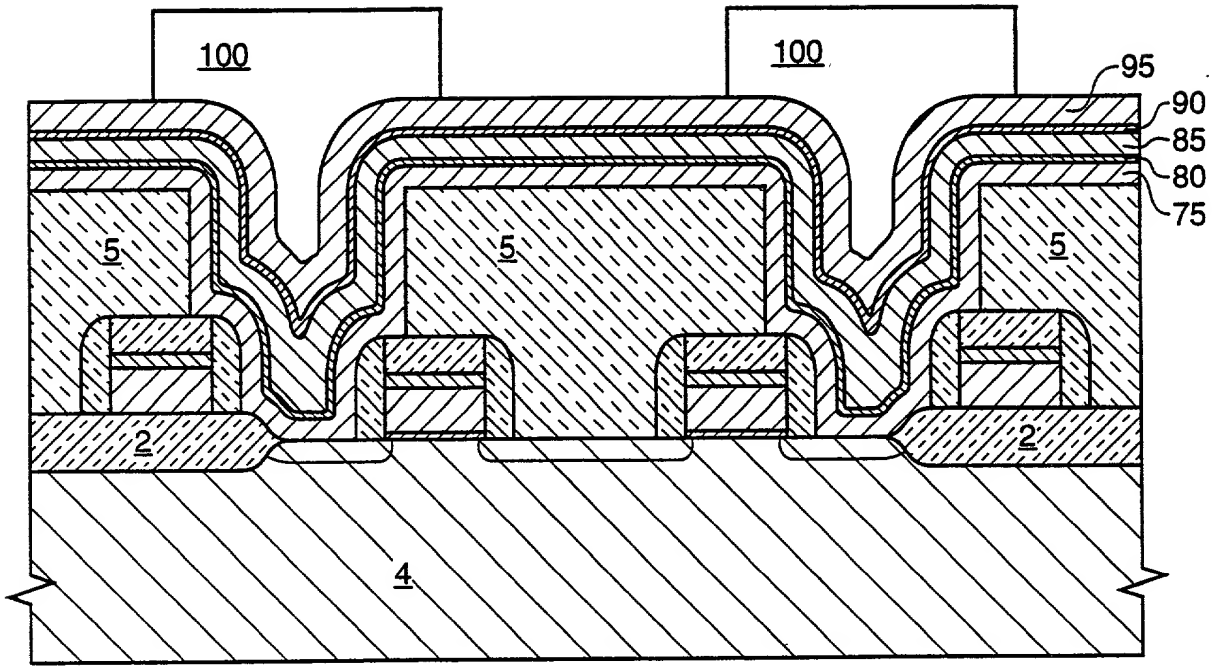

FIG. 11A

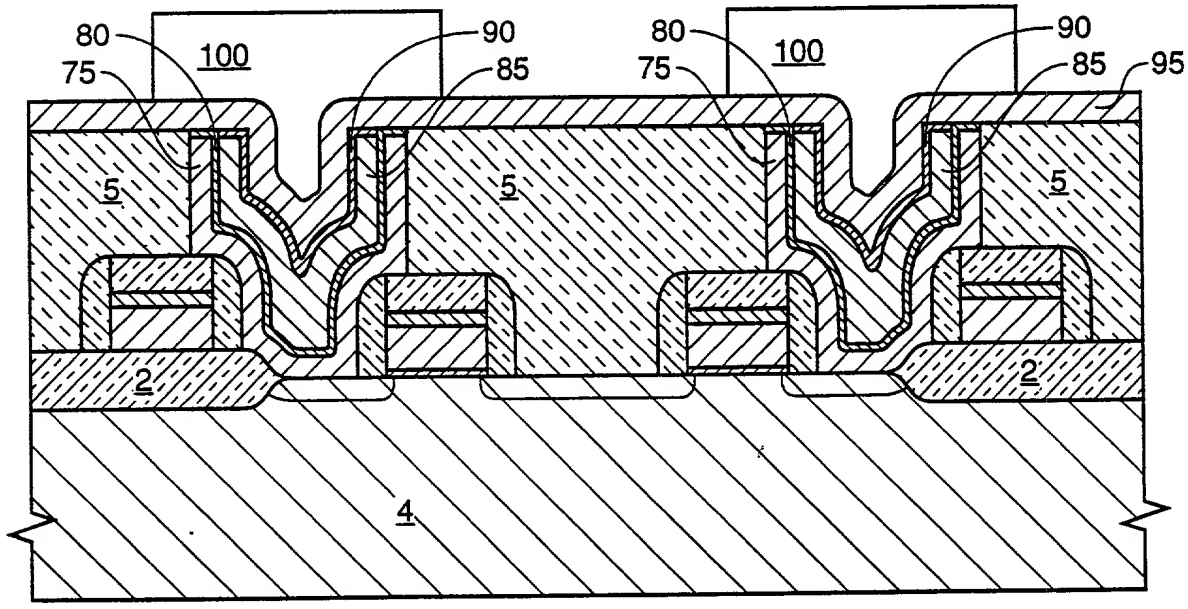

FIG. 11B

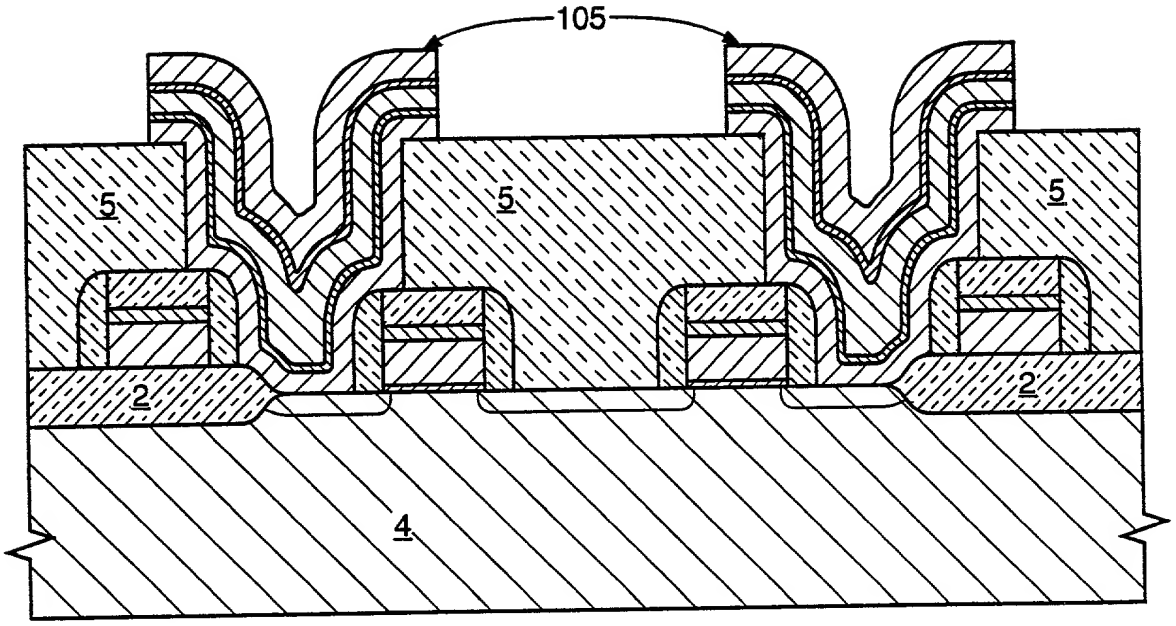

FIG. 12A

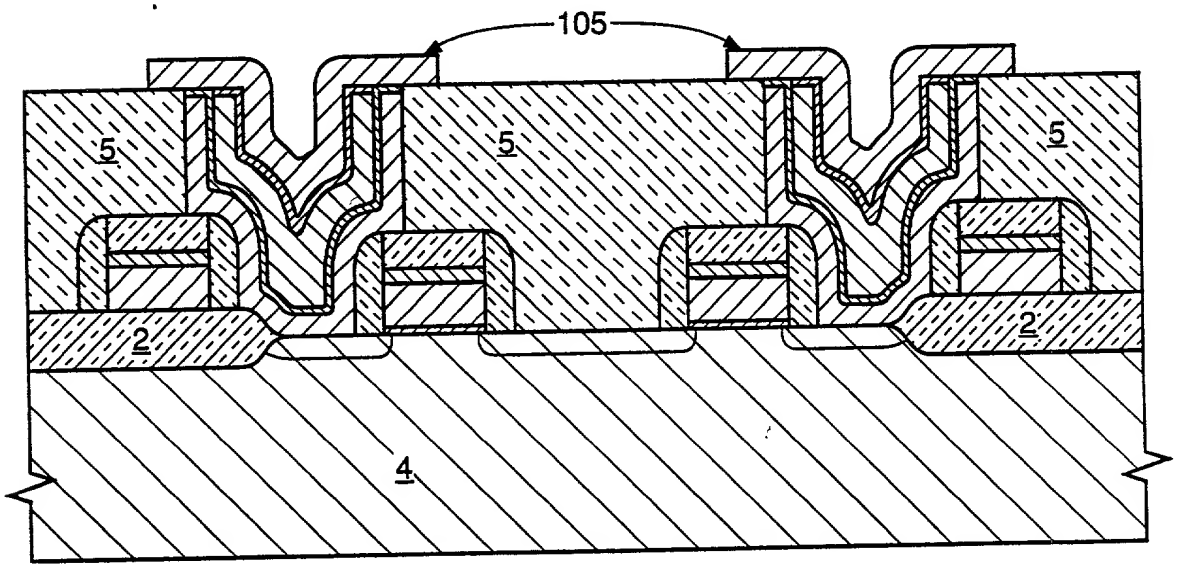

FIG. 12B

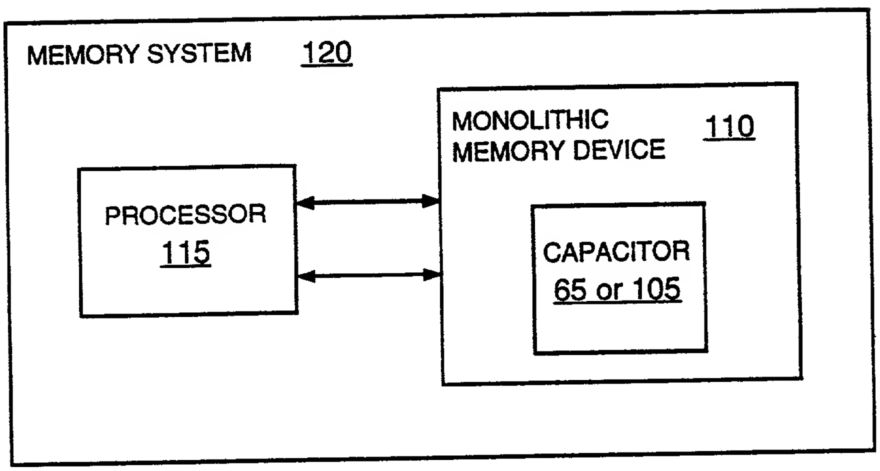
MEMORY SYSTEM 120
MONOLITHIC MEMORY DEVICE 110
PROCESSOR 115
CAPACITOR 65 or 105

FIG. 13

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Karl M. Robinson	Examiner: Unknown
Serial No.:	08/676,708	Group Art Unit: 2511
Filed:	July 8, 1996	Docket: 303.455US1
Title:	DEVICES HAVING IMPROVED CAPACITANCE AND METHODS OF THEIR FABRICATION	

REVOCATION AND POWER OF ATTORNEY

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

In accordance with 37 C.F.R. Section 1.36, M.P.E.P. Section 402.05, 402.07, and 324 please revoke any existing Powers of Attorney, if any, and appoint the following attorneys and/or patent agents to prosecute this application and to transact all business in the Patent and Trademark Office in connection therewith:

Bianchi, Timothy E.	Reg. No. 39,610	Holloway, Sheryl S.	Reg. No. 37,850
Billig, Patrick G.	Reg. No. 38,080	Klima-Silberg, Catherine I.	Reg. No. 40,052
Billion, Richard E.	Reg. No. 32,836	Kluth, Daniel J.	Reg. No. 32,146
Brennan, Thomas F.	Reg. No. 35,075	Lemaire, Charles A.	Reg. No. 36,198
Brooks, Edward J., III	Reg. No. 40,925	Lundberg, Steven W.	Reg. No. 30,568
Clark, Barbara J.	Reg. No. 38,107	Lynch, Michael L.	Reg. No. 30,871
Drake, Eduardo E.	Reg. No. 40,594	Madrid, Andres N.	Reg. No. 40,710
Dryja, Michael A.	Reg. No. 39,662	Pappas, Lia M.	Reg. No. 34,095
Embretson, Janet E.	Reg. No. 39,665	Schwegman, Micheal L.	Reg. No. 25,816
Farney, W. Bryan	Reg. No. 32,651	Simboli, Paul B.	Reg. No. 38,616
Fogg, David N.	Reg. No. 35,138	Slifer, Russell D.	Reg. No. 39,838
Forrest, Bradley A.	Reg. No. 30,837	Viksnins, Ann S.	Reg. No. 37,748
Harris, Robert J.	Reg. No. 37,346	Woessner, Warren D.	Reg. No. 30,440
Hofmann, Rudolph P., Jr.	Reg. No. 38,187		

Serial Number: 08/676,708
Filing Date: July 8, 1996
Title: DEVICES HAVING IMPROVED CAPACITANCE AND METHODS OF THEIR FABRICATION

CERTIFICATE UNDER 37 CFR §3.73(b)

Micron Technology, Inc. hereby certifies that it is the assignee of the entire right, title and interest in the patent application identified above by virtue of an assignment from the inventor filed July 8, 1996 and recorded on Reel 8090, Frames 0680 . To the best of my knowledge and belief, title is in the assignee, Micron Technology, Inc..

Pursuant to 37 C.F.R. §3.73(b) I hereby declare that I, Michael L. Lynch, am empowered to sign this certificate on behalf of the assignee, Micron Technology, Inc..

I hereby declare that all statement made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true.

Please direct all correspondence in this case to:

Schwegman, Lundberg, Woessner & Kluth, P.A.
P.O. Box 2938
Minneapolis, MN 55402
Telephone No. (612)373-6900

Date [illegible] By [signature]

Michael L. Lynch
Title:Chief Patent Counsel

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled [insert title of invention], the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37 of the Code of Federal Regulations, Section 1.56.

I hereby claim the benefit of any earlier filing date in the United States to which I am entitled under Title 35 of the United States Code, §120 and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35 of the United States Code, Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37 of the Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

Michael L. Lynch	Registration No. 30,871
Kevin D. Martin	Registration No. 37,882
Susan B. Collier	Registration No. 34,566
Lia M. Pappas	Registration No. 34,095
David J. Paul	Registration No. 34,692
Walter D. Fields	Registration No. 37,130
W. Eric Webostad	Registration No. 35,406

Send correspondence to: Susan B. Collier, Patent Agent
Micron Technology, Inc.
8000 S. Federal Way
Boise, Idaho 83706

Direct telephone calls to: Susan B. Collier
(208) 368-4514

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Title 18 of the United States Code, Section 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor: Karl M. Robinson
(First, Middle Initial, Last)

Inventor's Signature: _____ Date: 7/6/04

Residence
City, State, Country: Boise, Idaho United States of America

Citizenship: USA

Post Office Address: HC33, Box 1333
(if different from residence address) Boise, Id 83706